MATERIAL LIST

TOTAL SHEETS 1

FOR

REVISION X

TMC MODEL - BMA442

TITLE- CUST. SPEC. MOD. PKG

KIT 381
AUTOMATIC H.V. RECYCLE
will use some of the
drawings and material
contained on this
list..

USED ON MODEL -
MCTM-10KE

CONSISTS OF SUPPORTING LISTS

A-4846
refer to Mr Nieder

LAST SYMBOLS

P915
W902

MISSING SYMBOLS

J2006
P2006
W2003
A3003
J3005
S3003
W3003
XA3003

COMPILED B. Napierkowski
CHECKED _____
ENG APPR _____
FNL APPR _____
ISS DATE _____

ENGINEERING JOB NUMBER
E _____ - _____

§ FOR SPECIAL NOTES, REFER TO S1200.

MATERIAL LIST

PART NUMBER	DESCRIPTION	USED ON	QUANTITY	QUANTITY PER UNIT	REFERENCE SYMBOLS	SPECIAL NOTES REFER TO S 1200
A-4846	ASSY,PC BD	BMA442	1	1*	A3003	1
CA1587	CBL,SPCL PRP	BMA442	1	1*	W3003	
CK1838	DIAG,SCHEM,OVLD RESET	BMA442	1	1*		
CK1842	DIAG,SCHEM,MOD	BMA442	1	1*		
ID389	INST DWG,BMA442	BMA442	1	1*		
JJ172	CONN,RECP,BNC	BMA442	1		J3005	
		BMA442	1	2*	J2006	
JJ319-22DFE	CONN,RECP,PC	CA1587	1	1*	XA3003	
LA107-9-EXT IF	SLV,MKR,CBL	BMA442	1	1*		
LA107-9-J2006	SLV,MKR,CBL	BMA442	2	2*		
LA107-9-J3005	SLV,MKR,CBL	BMA442	1	1*		
LA107-9-P915	SLV,MKR,CBL	BMA442	1	1*		
LA107-9-P2006	SLV,MKR,CBL	BMA442	1	1*		
MS2665-20	BRACKET	BMA442	2	2*		
PC579	BD,PC	A-4846	1	1*		
PL244-1	CONN,PL,BNC	BMA442	1		P915	
		BMA442	1	2*	P2006	
RG174*/U	CBL,COAX	BMA442	1		W902	
		BMA442	1	2*	W2003	
ST103-5-62	SW,TOGGLE,SPST	BMA442	1	1*	S3003	
TE0135-28	SPCR,THD	BMA442	2	2*		

FOREWORD

This H.F. Linear Amplifier, model HFLM-10K is equipped with an Automatic Overload Reset Unit. This unit is optional and provided as per customer requirement. The Reset Unit provides automatic overload resetting of the transmitter.

Operation of the Reset Unit consists of setting a single switch to its on position. The RESET ON/OFF switch is located on the rear of the transmitter Input Chassis. Theory of Operation, schematic diagram, together with interconnecting drawing and parts list are provided as technical information.

Transmitter Automatic Reset Circuit

Theory of Operation

Ref: CK-1838

The transmitter automatic reset circuit is provided for automatic overload reset operation. It has the capability of being set for two (2) thru eight (8) overload resets. When the amount of overloads encountered within a predetermined period of time reaches the maximum number selected, the reset circuit will remain in a static condition keeping the transmitter in an overload condition. The automatic overload circuit is cleared by setting the HV ON-OFF switch to OFF.

Power to the reset circuit is provided by the transmitter being controlled. The reset circuit can be defeated simply by removal of the +24 VDC supply line. +24 VDC is necessary to operate the timing circuits and the relay driver circuits. By use of series resistor R1 and zener CR1 +5 VDC is developed for the operation of the IC's. Latching relay K2 is provided as an additional protect for automatic operation, to remove power from the reset card.

Transistors Q1, Q7, Q8 and unijunction Q2 comprise the automatic reset timing circuit. Transistors Q3, Q4, Q5 and unijunction Q6 comprise the counter clear timing circuit.

Integrated circuits Z1, Z4 and Z5 contain the logic gates necessary for control. Z2 is a BCD counter and finally Z3 is a BCD to decimal converter. Transistors Q11, Q10 and Q9 with relay K2 comprise the addition protect necessary during the initial power ON condition of the transmitter.

Initial Counter Clear Circuit:

When power is switched On, C5 will charge to +5 volts through R20. Q5 goes into saturation at the same time, resulting in a logic "0" or low (OV) on pin 1 of Z1D. This low is inverted to a high to pin 4 of Z1C. The combined gating action at Z1C results in a momentary high out of Z1C pin 6. This high will be present for the amount of time it takes for C5 to charge to +5V, after which the level will drop to a low. The momentary high presented to pins 2 and 3 of BCD counter (Z2) will "clear" the counter and insure that the counting sequence always starts from zero (0).

This initial clear pulse will also be seen through Z5B, Z5D, Z4D, and will arrive at pin 4 of Z4C as a momentary low. The momentary low on Z4C pin 4 will then be inverted to a high to pin 10 of Z4B. Pin 9 of Z4B will be at a high and the coincidence of both highs will cause a low out of Z4B. As this low is fed back into Z4C a "latch" will result with Z4C remaining high and Z4B remaining low. Z4A then presents a high to Q3. This will

forward bias Q3 on, resulting in Q4 being reversed biased keeping it cut off. With Q4 cut off, power is removed from the counter clear timing circuit.

Automatic Reset Timing Circuit:

The automatic timing circuit normally has power removed by the action of the ground from the reset condition of the overload relay in the transmitter. CR2 and CR3 form an "OR" circuit to control transistor switch Q1. A logic high on CR2 or CR3 will turn Q1 on. When an overload occurs in the transmitter, ground is lifted from CR2. +24 volts will then be seen through R5 to CR2 which will forward bias Q1 on. Supply voltage is now supplied to the reset timing circuit. Q7 will turn on due to the positive voltage thru R3 to its base. C3 will begin to charge because of the potential difference across it from R2 (+) to base of Q7 (-). C3 will continue to charge until the threshold voltage of Q2 has been reached. When the threshold voltage of Q2 is exceeded, the unijunction will "fire" providing a discharge path for C3. When the unijunction (Q2) is triggered, a 150 msec pulse is developed. This pulse is coupled through relay driver Q8 to K1. K1 will energize and reset the overload condition in the transmitter. With the transmitter overload reset, CR2 will be grounded again.

In order to insure proper relay operation for the pulse duration, +24V is fed back to CR3 by normally open contacts of K1. Q1 will remain on until K1 has dropped out. Power is then removed from the reset timing circuit. When an additional overload occurs, the above sequence is repeated.

Overload Reset Counting Circuit:

R13, R14, Z1A and Z1B monitor the operation of K1. The contact bounce normally found with relays is removed by this circuit, insuring proper presentation of pulses to the BCD counter (Z2), count input. When K1 operates, the output of Z1B which is normally low will switch to a high. When K1 drops out the output of Z1B will return to a low. During the high to low transition of Z1B, BCD counter (Z2) output will change. The four line output (A, B, C, D) will change from all lows to a high on A and lows on B, C, and D. The four line output will follow a binary format with A, B, C and D displaying binary 1, 2, 4, and 8 respectively. The binary counter output will change for each overload reset operation. If the maximum amount of overloads has not been reached in the prescribed time, and the transmitter is in the reset condition, Z2 (BCD counter) will be reset to zero (o).

Maximum Overload Detector Circuit:

B C D to Decimal Decoder (Z3) monitors the output of the B C D counter (Z2) and will have one low output for each B C D input for a total of ten (10) different outputs. A strap wire matrix is provided which enables the user to select two (2) thru eight (8) resets. When the maximum amount of resets have been reached the selected output will switch to a low. The low will be seen at CR2. CR3 input will be open; this combination will result in Q1 being reversed biased to cut off. Power will then be removed from the auto reset timing circuit. The overload relay in the transmitter will be in the overload condition. This condition will inhibit the counter clear timing circuit from clearing the B C D counter. The transmitter will be kept in the overload condition until the HV ON-OFF switch is set to OFF. This action will reset the overload relay and remove power from the automatic reset board by applying ground to the base of Q12. When the HV ON-OFF switch is set to On, proper operation is then resumed.

Counter Clear Timing Circuit:

Q4 is being kept "OFF" by the initial "ON" state of Q3 and the subsequent "latch" of Z4C and Z4B. In order to turn Q4 on, the "latch" must be reversed. This is accomplished as follows:

When K1 operates, the high from Z1A will switch to a low. This low is seen on pin 9 of Z4B. The output of Z4B will then swing high. As both inputs of Z1C are now high the output of Z1C will go low to keep Z1B output high. The "latch" has now been reversed. Z4A inverts the high to a low causing Q3 to be reversed biased to cut off. +24V will now be seen at the base of Q4 thru R6. The forward bias on Q4 drives it to saturation. Supply voltage is now applied to the clear timing circuit. Circuit operation will be the same as previously described for the auto reset timing circuit. When the threshold voltage of Q6 is exceeded the uni-junction will "fire" providing a discharge path for C4. This condition will reverse bias Q5 to cut off for a logic high at the output of Q5. A resulting pulse width of 15 msec is presented to Z1D pin 1. If Z1D pin 2 is not grounded by the overload relay in the transmitter, the 15 msec pulse will be seen through Z1C to the clear input of the B C D counter (Z2) and will clear the counter (all outputs will be low). The high from Q5 will arrive at Z4C as a low and will cause the latching circuit of Z4C and Z4B to reverse its logic levels (high out of Z4C and low out of Z4B). Q3 will now become forward biased and Q4 will cut off removing power from the clear timing circuit. R7 is used to provide sufficient current drain to keep Q4 in conduction during the charging sequence of the clear timing circuit.

"Protect" Circuit:

Q11 is monitoring the end of the interlock line. If 24V is missing for any reason on this line Q11 will switch a low to Q10, Q10 will go high and Q9 will switch low. This low will energize the trip coil of K2 and power will be removed from the reset circuit board. In order to restore power to the reset circuit board, the HV ON-OFF switch must be set OFF and then ON. This feature is used in cases where the transmitter is first turned on and the timer has not cycled. Another condition is when an interlock has been opened. The operator is compelled to reset the HV ON-OFF switch for proper operation. Finally, coming from pin 2 of Z3 (B C D to decimal decoder) is the "fail safe" line. This line comes into use in case the maximum overload detection circuit did not work. A low from this output will also cause the trip coil of K2 to energize removing power from the reset circuit board.

A-4846

TRANSMITTER AUTO RESET BD ASSY

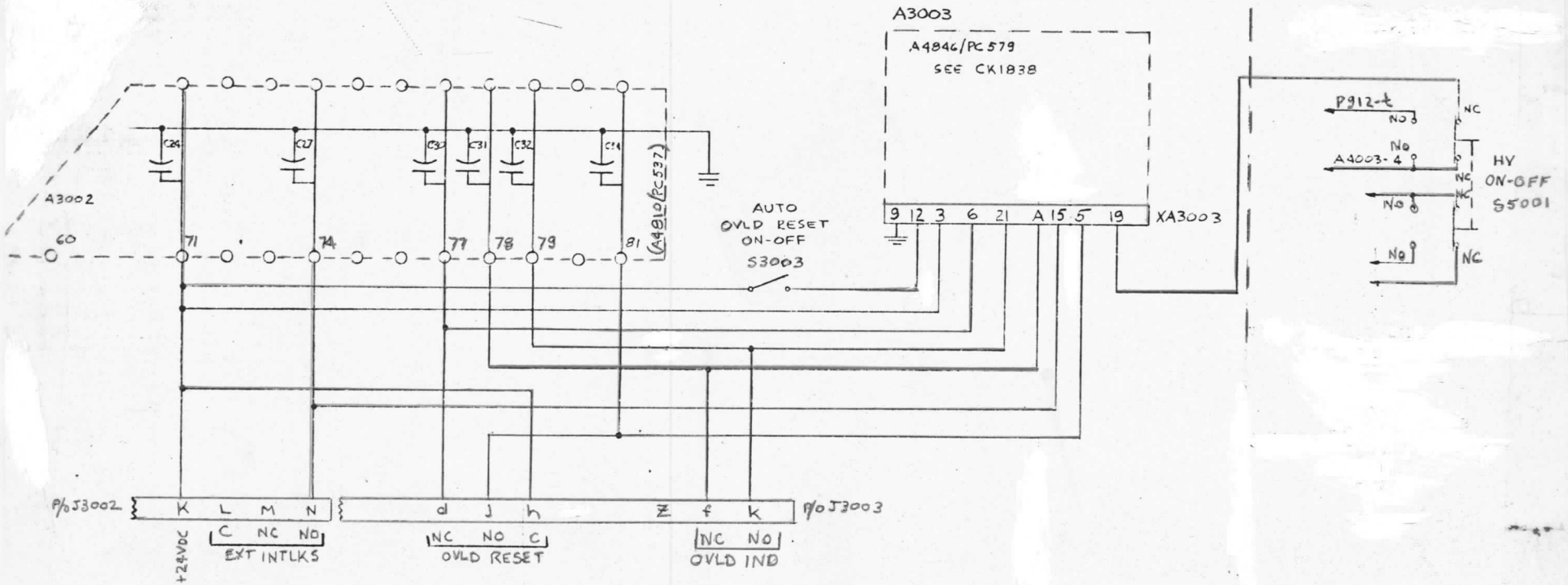
REF SYMBOL	DESCRIPTION	TMC PART NUMBER
C1	Capacitor	CX119-104M
C2	Same as C1	
C3	Capacitor, Fixed, Electrolytic	CE105-75-50
C4	Capacitor, Fixed, Electrolytic	CE105-20-50
C5	Capacitor, Fixed, Electrolytic	CE105-1-15
CR1	Semiconductor, Device, Diode	1N3826
CR2	Semiconductor, Device, Diode	1N914
CR3	Same as CR2	
CR4 thru CR7	Semiconductor, Device, Diode	1N270
K1	Relay, Armature	RL156-8
K2	Relay, Armature	RL156-9
Q1	Transistor	2N697
Q2	Transistor	2N492
Q3 thru Q5	Same as Q1	
Q6	Same as Q2	
Q7 thru Q11	Same as Q1	
Q12	Transistor	2N1485
R1	Resistor, Fixed, WW 150 ohms, 10W	RR116-150W
R2	Resistor, Fixed, Composition	RC07GF473J
R3	Resistor, Fixed, Composition	RC07GF472J
R4 thru R6	Same as R3	
R7	Resistor, Fixed, Composition	RC20GF222J
R8	Resistor, Fixed, Composition	RC20GF225J
R9	Resistor, Fixed, Composition	RC07GF102J
R10	Same as R9	
R11 thru R16	Same as R3	
R17	Same as R7	
R18	Resisistor, Fixed, Composition	RC07GF103J
R19	Same as R9	
R20	Same as R9	
Z1	IC Network	NW176
Z2	IC Network	NW174
Z3	IC Network	NW165
Z4	Same as Z1	
Z5	Same as Z1	

KIT 381

AUTOMATIC OVERLOAD RESET

REF SYMBOL	DESCRIPTION	TMC PART NUMBER
A3003	PC Board Assembly	A-4846*
S3003	Switch, Toggle SPST	ST103-5-62
XA3003	Connector, Receptacle, PC	JJ319-22-DFE
CK1838	Schematic Diagram (A4846)	

* Parts breakdown for this assembly supplied on a separate list.


A3003
A4846/PC579
SEE CK1838
A3002
60
71
74
77
78
79
81
C24
C27
C30
C31
C32
C14
(A4810/PC537)
AUTO
OVLD RESET
ON-OFF
S3003
9 12 3 6 21 A 15 5 19
XA3003
P912-t
NO
NC
A4003-4
HV
ON-OFF
S5001
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NC NO
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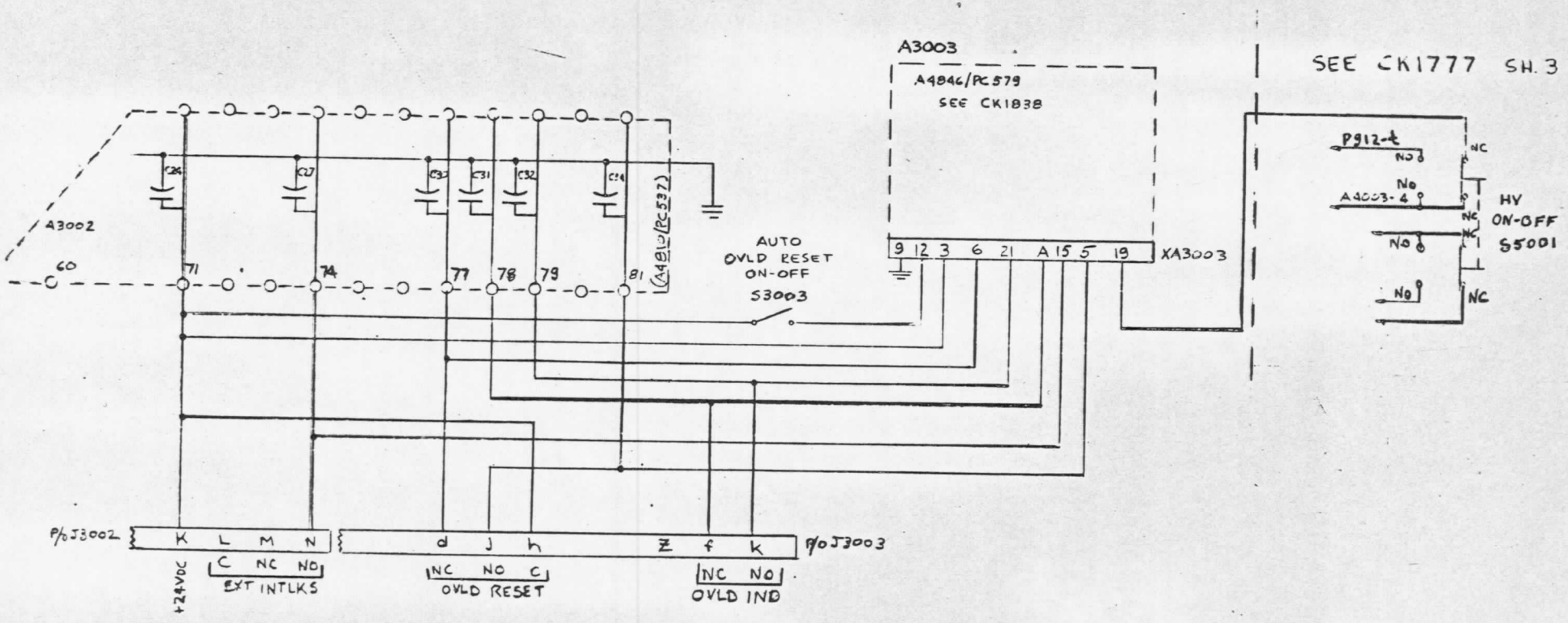

Automatic Reset Interconnecting Diagram