TMC SPECIFICATION

NO. S1409

REV:

COMPILED: R. Uzzo | CHECKED: | APPD: | SHEET OF

TITLE:

SERIAL NO.

PRODUCTION TESTING

(REFERENCE TEST SPECIFICATION)
SMA635374

TMC SPECIFICATION			NO. S1409
REV:			
COMPILED: R. Uzzo	CHECKED:	APPD:	SHEET OF
TITLE: CONTRACTOR TESTING			

1. GENERAL INFORMATION

a) CONTRACTOR - - - - - - - - - TECHNICAL MATERIEL CORP.
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

b) CONTRACT ORDER NUMBER - - DAAB07-81C-1108

c) NOMENCLATURE - - - - - - - - POST TRIGGER GENERATOR ASSEMBLY
P/O AN?TPX - 46
DRAWING NO. SM-D-586746
NSN # 5895-00-199-9685

(EQUIPMENTS OF ESTABLISHED DESIGN)

d) SMD586746 FABRICATED AT:
TECHNICAL MATERIEL CORP.
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

e) SMD586746 ASSEMBLY - - - - STOCK NO. REPRESENTED BY
SERIAL NO _____

f) TESTING LOCATION:
TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

g) TESTING DATE: _____

h) TEST SPECIFICATIONS - SM-A-635374

2. CROSS REFERENCING TABLE FOR SPECIFICATION SMA635374

SPECIFICATION SMA635374 REFERENCE PARAGRAPH NO.	SPECIFICATION DESCRIPTION	PAGE	PARAGRAPH NO.
3.2.1.1	POWER REQUIREMENTS	4	3.4.3
3.2.1.2	SIGNAL REQUIREMENTS	4	3.4.2
3.2.1.2.7	LOAD REQUIREMENTS	4	3.4.4
3.2.2	$\overline{\text{RTA2}}$ MEASUREMENTS	5	4.1
		5	4.2
3.2.4	$\overline{\text{DATA LOCKOUT ENABLE}}$,	6	5.7
	$\overline{\text{DATA LOCKOUT}}$ MEASUREMENTS	6	5.8
		6	5.9
		6	5.14
		6	5.17
3.2.6	$\overline{\text{(MODE 4 + TEST TARGET)}}$ MEASUREMENTS	7	6.2
		7	6.5

3. PURPOSE

TO ASSURE THAT THE ESTABLISHED, ACCEPTANCE TESTING FOR THE POST TRIGGER GENERATOR ASSEMBLY IS IN ACCORDANCE WITH TEST REQUIREMENTS, SMA635374.

3.1 TEST EQUIPMENT USED (or equivalent)

a) CON AVIONICS REGULATED LV POWER SUPPLY, MODEL W32-5 TMC ID NO. 1921.

b) E-H RESEARCH LABORATORIES, PULSE GENERATOR MODEL MO139B. (CALIBRATION EXPIRES 7-6-83, CAL BY RAG CALIBRATION SERVICE
c) TEKTRONIX OSCILLOSCOPE TYPE 541A. (CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECTRIC)
d) HEWLETT PACKARD ELECTRONIC COUNTER MODEL 5245L. (CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECTRIC)
e) FLUKE MULTIMETER, MODEL 80208 SERIAL NO. 2801343 (CALIBRATION EXPIRES 7-5-83, CAL BY R & P ELECTRIC)

3.2 SPECIAL TEST CIRCUIT (ALL UNITS USED TO GENERATE INPUT SIGNALS TO THE TEST CIRCUIT ARE IN CALIBRATION, THE REQUIRED OUTPUT SIGNALS GENERATED BY THE TEST CIRCUIT ARE THE RESULT OF CALIBRATED INPUT SIGNALS.) TMC CONSTRUCTED THE TEST CIRCUIT, IN ORDER TO GENERATE THE REQUIRED INPUT SIGNALS TO THE SMD586746 ASSEMBLY. (SEE FIGURE 1-1)

3.3 REFERENCE DATA USED

a) SMA635374 (TEST SPECIFICATIONS)

b) SMD586746 (ASSEMBLY DRAWINGS)

c) SME586846 (SCHEMATIC DIAGRAM)

d) TMC TEST CIRCUIT (SCHEMATIC DIAGRAM - FIGURE 1-1 PAGE 8

3.4 TMC-PREPARED TEST CIRCUIT (SCHEMATIC FIGURE 1-1)

TMC HAS PREPARED A TEST CIRCUIT TO GENERATE THE REQUIRED INPUT SIGNALS NECESSARY IN TESTING THE POST TRIGGER GENERATOR ASSEMBLY. THIS TEST CIRCUIT IS HOUSED IN A .063 ALUM ALY CHASSIS 12 INCHES LONG BY 7 INCHES WIDE AND 2 INCHES DEEP. A PRINTED WIRING BOARD WAS CONSTRUCTED TO HOUSE THE CIRCUITS COMPONENTS, FIGURE 1-1 GIVES A SCHEMATIC REPRESENTATION OF THE TEST CIRCUIT. ALL COMPONENT VALUES USED IN THE TEST CIRCUIT ARE CALLED OUT IN THE SCHEMATIC DIAGRAM (FIGURE 1-1), AND ARE FOUND ADJACENT TO ALL COMPONENT SYMBOLS.

3.4.1 THE FOLLOWING ARE INPUTS DEVELOPED BY TMC'S TEST CIRCUIT.

INPUT PIN	INPUTS DEVELOPED
10	PULSE: NEGATIVE POLARITY: .05uS < PW < .8uS: PRF: 300 PPS
16	PULSE: NEGATIVE POLARITY: 0.05uS < PW < 0.4uS: POSITION: 15 to 20 uS BEFORE THE LEADING EDGE (LE) OF THE PULSE AT INPUT PIN 10.
8	PULSE: NEGATIVE POLARITY: 0.5uS < PW < 1.5uS POSITION: 400 to 475uS BEFORE THE LE OF THE PULSE AT INPUT PIN 10.
34	SQUARE WAVE 0.10uS PERIOD.

3.4.2 SIGNAL REQUIREMENTS

PIN VARIES	HIGH LEVEL (LOGIC "1") VOLTAGE DEVELOPED BETWEEN +2.4VDC AND +5.25VDC.
PIN VARIES	LOW LEVEL (LOGIC "0") VOLTAGE DEVELOPED BETWEEN 0-0.5VDC AND 0+0.5VDC.

3.4.3 POWER REQUIREMENTS

PIN 1 AND 40	VOLTAGE APPLIED +5.±0.25VDC
PIN 2 AND 41	VOLTAGE GROUND RETURN

3.4.4 OUTPUT LOADING

THE FOLLOWING RESISTORS ARE CONNECTED AT THE OUTPUT PINS (SPECIFIED) AND +5±0.25VDC- TO ACCOMPLISH LOADING.

OUTPUT PIN	RESISTOR VALUE	LOGIC "0" LOAD	LOGIC "1" LOAD
3	2.7K	1.6 MA	40 uA
19	470 OHM	9.6 MA	320 uA
24	2.7K	1.6 MA	40 uA
22	2.7K	1.6 MA	40 uA

(SEE CHART 1-1 PAGE 9)

3.4.5 CONNECT A JUMPER FROM OUTPUT PIN 6 TO TERMINAL "K" OF THE TEST CIRCUIT.

3.4.6 CONNECT A JUMPER FROM OUTPUT PIN 38 TO TERMINAL "L" OF THE TEST CIRCUIT.

3.4.7 CONNECT A JUMPER FROM INPUT 36 TO TERMINAL "J" OF THE TEST CIRCUIT.

REFERENCE

3.4.8 SCHEMATIC DIAGRAM SM-E-586846

MAKE CONNECTIONS AS SHOWN ON SCHEMATIC DIAGRAM SM-E-586846, U17.

4. RTA2 TEST

4.1 MEASURE BETWEEN OUTPUT PIN 19 AND INPUT PIN 18 - - - A SHORT CIRCUIT (1 OHm MAXimum)

4.2 MEASURE BETWEEN OUTPUT PIN 22 AND INPUT PIN 21 - - - A SHORT CIRCUIT (1 OHm MAXimum)

5. DATA LOCKOUT ENABLE, DATA LOCKOUT TEST

5.1 CONNECT A JUMPER FROM INPUT PIN 10 TO TERMINAL "E" ON THE TEST CIRCUIT. TERMINAL "E" IS A NEGATIVE POLARIZED PULSE BETWEEN .05uS < PW < .8uS PRF: 300 PPS

5.2 CONNECT A JUMPER FROM INPUT PIN 16 TO TERMINAL "F" ON THE TEST CIRCUIT. TERMINAL "F" IS A NEGATIVE POLARIZED PULSE BETWEEN .05uS < PW < 0.4uS
POSITIONED: 15 TO 20uS BEFORE THE LEADING EDGE (LE) OF THE PULSE AT INPUT PIN 10 (MONITOR PIN 16 ON THE OSCILLOSCOPE USING THE DIRECT TRIGGER INPUT EXT. TRIGG (-) AND CHAN "B" PROB, CHAN "A" PROB ON PIN 10, MODE TO BE ALT (5uS SCALE)

5.3 CONNECT A JUMPER FROM INPUT PIN 8 TO TERMINAL "A" ON THE TEST CIRCUIT. TERMINAL "A" IS A NEGATIVE POLARIZED PULSE BETWEEN .5uS < PW < 1.5uS
POSITIONED 400 TO 475uS BEFORE THE LE OF THE PULSE AT INPUT PIN 10. MONITOR PIN 8 ON THE OSCILLOSCOPE USING THE DIRECT TRIGG INPUT EXT. TRIGGER (-) AND CHAN "B" PROB, CHAN "A" PROB ON PIN 10, MODE TO BE ALT (.1MS SCALE)

5.4 CONNECT A "LOGIC 1" JUMPER TO INPUT 4

5.5 CONNECT A "LOGIC 1" JUMPER TO INPUT 17

5.6 CONNECT A "LOGIC 0" JUMPER TO INPUT 26

5.7 OUTPUT PIN 3 MEASURES - - - - - - - - - - - - - HIGH LEVEL

5.8 OUTPUT PIN 6 MEASURES - - - - - - - - - - - - - A WAVEFORM WHICH GOES LOW AT THE TRAILING EDGE (TE) OF THE PULSE AT INPUT PIN 16.

ON THE OSCILLOSCOPE (CHAN A=PIN-16, CHAN B=PIN 6, DIRECT TRIGG EXT (-) PIN-6, (.2u Sec) (ALT MODE)

5.9 OUTPUT PIN 6 MEASURES - - - - - - - - - - - - - A WAVEFORM WHICH GOES HIGH AT THE LE OF THE PULSE AT INPUT PIN 10

ON THE OSCILLOSCOPE CHAN A=PIN-10, CHAN B=PIN 6, DIRECT TRIGG EXT (-) PIN 6 (5u Sec) (ALT MODE)

5.10 REMOVE THE INPUT JUMPERS TO PINS 8, 16 AND 17.

5.11 CONNECT A JUMPER FROM INPUT PIN 34 TO TERMINAL "G" OF THE TEST CIRCUIT. TERMINAL "G" IS A SQUARE WAVE, .10us PERIOD.

5.12 REMOVE THE "LOGIC 0" JUMPER TO INPUT PIN 26.

5.13 CONNECT A "LOGIC 1" JUMPER TO INPUT PIN 26

5.14 OUTPUT PIN 38 MEASURES A PULSE WITH THE FOLLOWING CHARACTERISTICS:

POLARITY Positive (INT. TRIGG +)

PULSE WIDTH .05uS TO 1.5 uS

AMPLITUDE 1.0 VOLT MINIMUM } ON OSCILLOSCOPE .2V SCALE = 2V

NEGATIVE OVERSHOOT 2.0 Volts MAX

POSITION WITH IN 0.5 us of the LE of The PULSE AT INPUT PIN 10

ON THE OSCILLOSCOPE (.5V SCALE) MODE ALT (.5uS)

5.15 REMOVE THE "LOGIC 1" JUMPER TO INPUT PIN 26

5.16 CONNECT A "LOGIC 0" JUMPER TO INPUT PIN 26

5.17 OUTPUT PIN 38 MEASURES A PULSE WITH THE FOLLOWING CHARACTERISTICS:

POSITION: 460 ± 20us BEFORE the (LE) of THE →

5.17 POSITION: (CONTINUED)

PULSE AT INPUT PIN 10

ON THE OSCILLOSCOPE USE INPUT TRIGGER DIRECTLY EXT TRIGG (+) AND PROB "B" ON PIN 38, PROB A ON PIN 10, .2MS SCALE.

6. (MODE 4 + TEST TARGET) ENABLE TEST

6.1 CONNECT A "LOGIC 0" JUMPER TO INPUT PIN 28.

6.2 OUTPUT PIN 24 MEASURES HIGH LEVEL

6.3 REMOVE THE "LOGIC 0" JUMPER TO INPUT PIN 28.

6.4 CONNECT A "LOGIC 1" JUMPER TO INPUT PIN 28.

6.5 OUTPUT PIN 24 MEASURES LOW LEVEL

6.6 DISCONNECT ALL INPUTS.

END OF TESTS

ALL TEST REQUIREMENTS FOR THE POST TRIGGER GENERATOR ASSEMBLY SMD586746 HAVE BEEN COMPLIED WITH, IN ACCORDANCE WITH "TEST REQUIREMENTS SIF SIF SMA635374."

ALL TEST PROCEDURES SPECIFIED IN THIS TEXT WILL BE IMPLEMENTED DURING TESTING OF ALL SMD586746 ASSEMBLIES.

DATE TEST WAS PERFORMED _____

TESTERS SIGNATURE _____ SERIAL NO. _____

WITNESSED BY

GOVERNMENT REPRESENTIVE _____

DATE _____